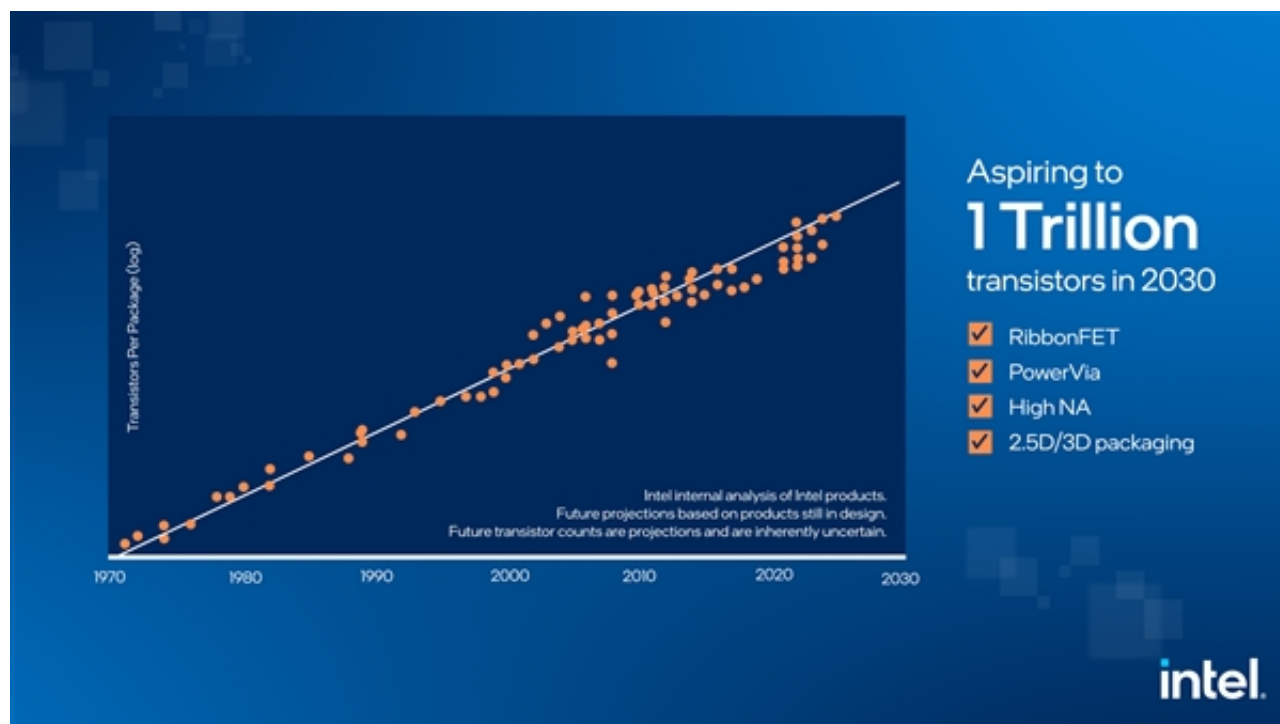
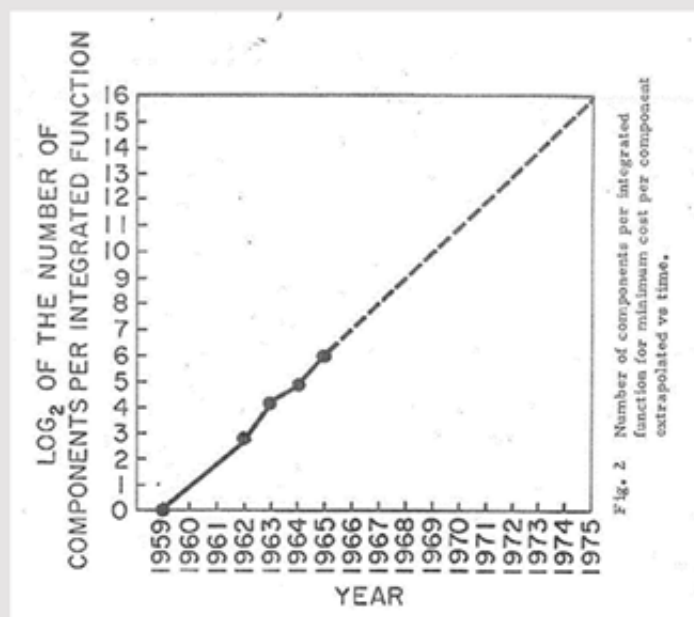


Intel目标2030年做到单芯片集成1万亿个晶体管

晶体管的数量/密度一直是衡量半导体技术进步的重要指标。目前单个芯片上可以实现超过1000亿个晶体管，比如Intel Ponte Vecchio GPU。在IEDM 2022 IEEE国际电子设备大会上，英特尔宣布了多项新的技术突破，并将继续执行已经诞生75年的摩尔定律。目标是到2030年在单个芯片上集成1万亿个晶体管，是现在的10倍。

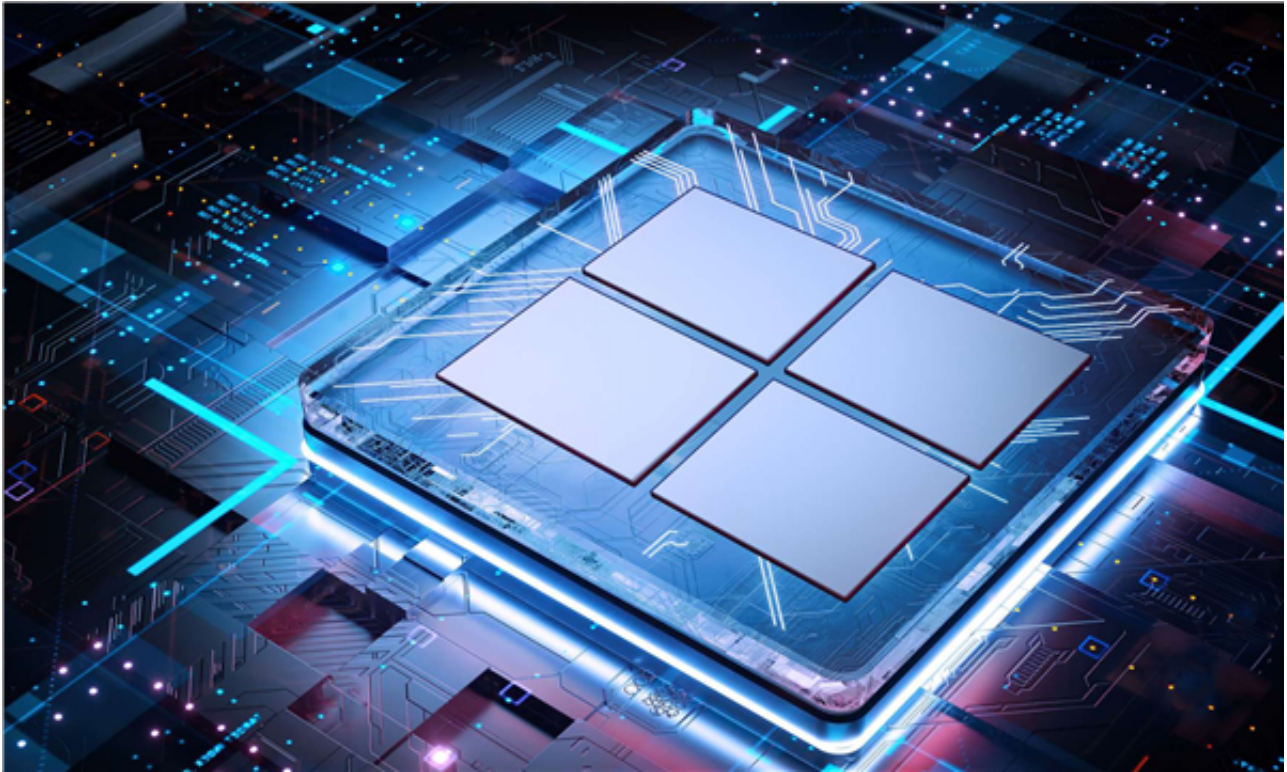




摩尔定律原型

从应变硅、高K金属栅极、FinFET立体晶体管，到未来的RibbonFET GAA环绕栅极晶体管、PowerVia后置供电，再到2.5D EMIB + 3D Foveros、Foveros Direct/Omni封装技术，Intel一直在从各项技术上推动摩尔定律。

IEDM 2022会议上，Intel披露了三个方面的技术突破：

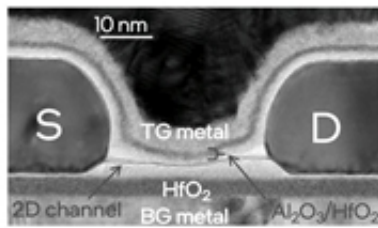


1、下一代3D封装准单芯片

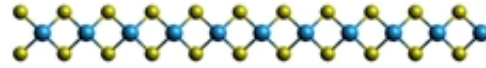
基于混合键合(hybrid bonding)，将集成密度和性能再提升10倍。

同时，间距缩小到3微米，使得多芯片互连密度和带宽媲美如今的单芯片SoC。

Moore's Law scaling beyond Si with 2D materials

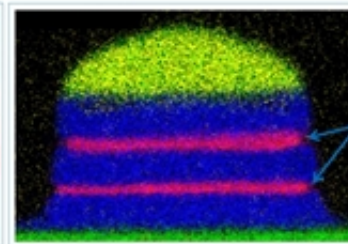
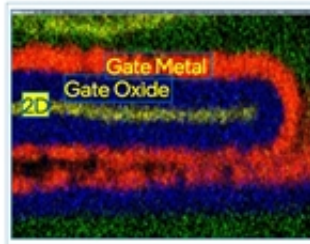


3 atoms thick



Super thin novel channel material to replace Si

- Scaled 2D device fabrication – approaching Si state-of-the-art dimensions
- Specialized gate oxide growth for 2D surfaces achieves near ideal subthreshold slope (SS)



2D nanosheet stacking

Paper #7.5: Gate length scaling beyond Si: Mono-layer 2D Channel FETs Robust to Short Channel Effects

intel

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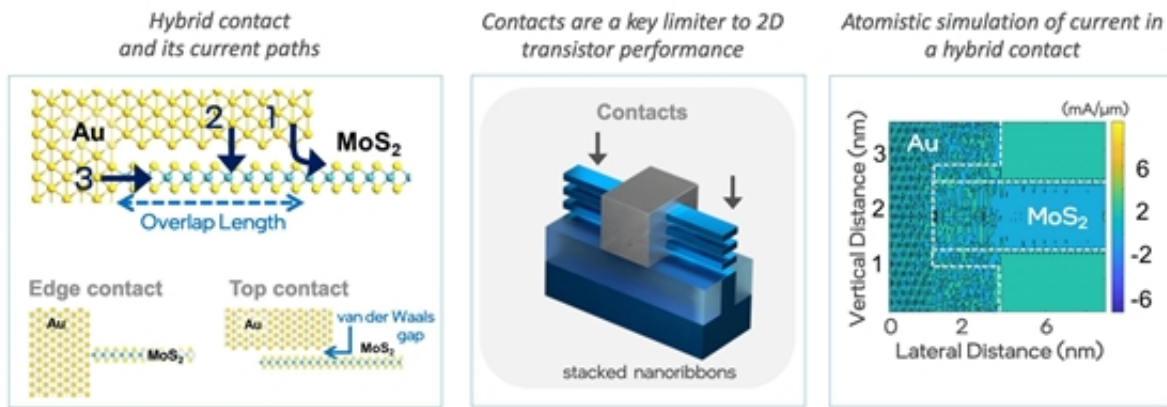
2、超薄2D材料在单芯片内集成更多晶体管

使用厚度仅仅3个原子的2D通道材料，Intel展示了GAA堆栈纳米片，在双栅极结构上，在室温环境、低漏电率下，达成了非常理想的晶体管开关速度。

第一次深入揭示了2D材料的电接触拓扑，可实现更高性能、更有弹性的晶体管通道。

Enabling the engineering of contacts to 2D channel materials

First comprehensive set of numerical and analytical models of 2D contacts



Atomistic simulations show paths to high performing contacts for 2D transistors

Paper #28.5: Characterization and Closed Form Modeling of Edge/Top/Hybrid Metal- 2D Semiconductor Contacts

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3、高性能计算能效、内存新突破

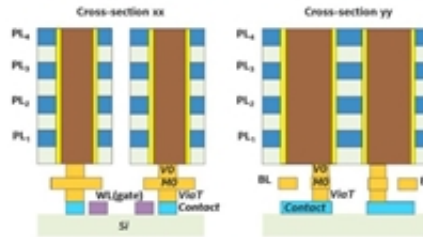
Intel研发了可垂直堆叠在晶体管之上的全新内存，并首次展示了全新的堆叠铁电电容，性能媲美传统铁电沟道电容，可用于在逻辑芯片上打造FeRAM。

Intel正在打造300毫米直径的硅上氮化镓晶圆，比标准的氮化镓提升20倍。

Intel在超高能效方面也取得了新的突破，尤其是晶体管在断电后也能保存数据，三道障碍已经突破两道，很快就能达成在室温下可靠运行。

First demonstration of 3D stacked capacitors for FeRAM density

- At IEDM 2020, Intel presented 3D FeRAM concept
- Breakthrough in 1T-1C FeRAM scaling by stacking (Anti)-ferroelectric capacitors.
- Research for the future of embedded memory



IEDM 2022 marks industry's first demonstration of stacked array capacitors with matched performance to conventional ferroelectric trench capacitors.

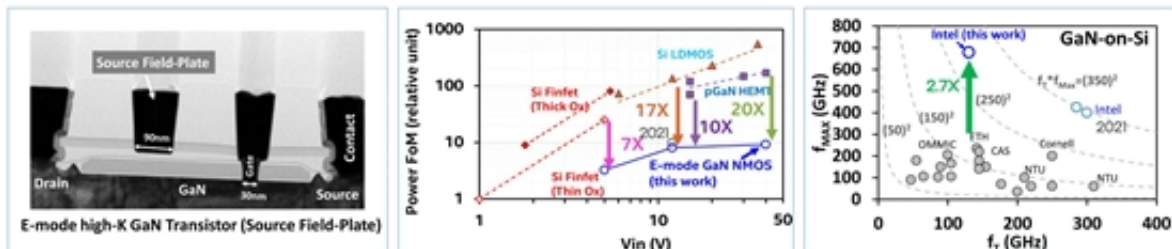


Paper #6.7: Hafnia-Based FeRAM: A Path Toward Ultra-High Density for Next-Generation High-Speed Embedded Memory

Major advancement in 300mm GaN-on-Si technology

Enabling silicon to keep pace with power and performance demands

Industry record Figure-of-Merit for power switches and RF transistors

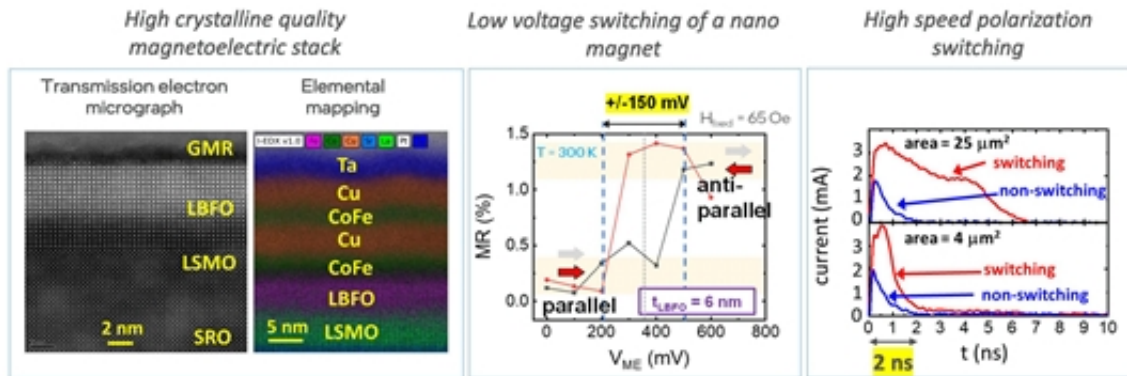


- 20x gain (resistance times charge) over industry standard GaN
 - Industry best Figure-of-Merit for high-performance power delivery
- Record cut-off frequency, f_{MAX} of 680GHz for 5G and beyond
- Viable path to 300mm GaN-on-silicon wafers

Paper #35.1: Scaled Submicron Field-Plated Enhancement Mode High-K Gallium Nitride Transistors on 300mm Si(111) Wafer with Power FoM (RONxQGG) of 3 mohm-nC at 40V and f_T/f_{MAX} of 130/680GHz

Super energy efficient technology for logic and memory

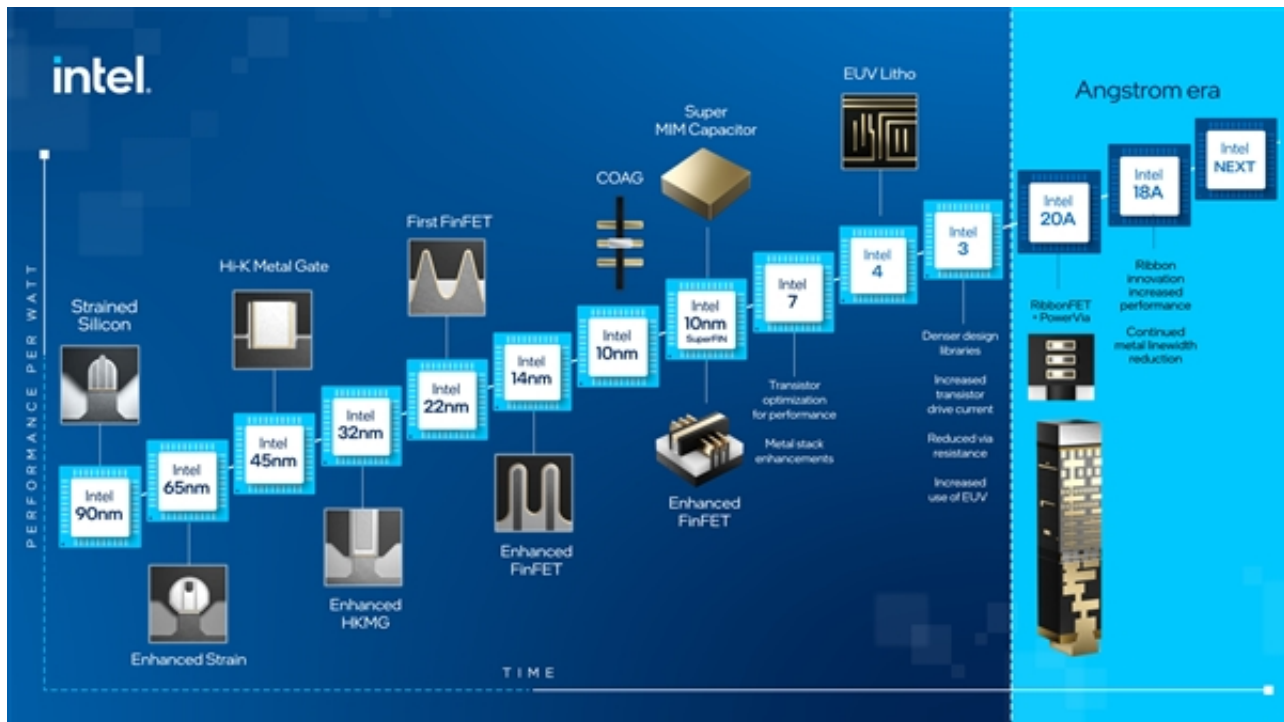
Low voltage and high-speed switching of magneto electric device



- 150 mV voltage-driven switching of a ferromagnet exchange-coupled to lanthanum-doped BiFeO₃ (LBFO) at room temperature
- Less than 2 ns switching of LBFO ferroelectric polarization at room temperature
- These two results are respectively the lowest voltage magneto electric switching and the highest switching speed measured in LBFO, enabled by high quality epitaxial growth of ultra-thin LBFO/FM films

Paper #36.4: Low voltage and high-speed switching of a magneto electric element for energy efficient compute

intel 15



Intel制造工艺路线图



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